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Claim 1 (currently amended): A method for fabricating a silicon based package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface; [[,]]

then forming a protective overcoat layer over the interconnnection structure; [[, and]]

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure; [[,]]

then thinning the reverse surface of the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP; [[,]]

then forming via holes which extend through the UTSW; [[,]]

then forming metallization in the via holes with the metallization extending through the UTSW; and

then ~~remove~~ removing the temporary bond.

Claim 2 (previously presented): The method of claim 1 including bonding the metallization in the via holes to pads of a carrier.

Claim 3 (previously presented): The method of claim 1 including forming capture pads on the first surface prior to thinning the wafer.

Claim 4 (currently amended): The method of claim 1 including:

initially forming capture pads on the first surface; [[,]]

then forming the interconnection structure over the first surface and the capture pads; [[,]]

then forming the temporary bond of the wafer holder to the reverse surface; [[,]] and

then thinning the wafer, thereby forming the UTSW.

Claim 5 (currently amended): The method of claim 1 including:

initially forming capture pads on the first surface; [[,]]

then forming interconnection structure over the first surface and the capture pads; [[,]]

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW; [[,]] and

then forming the via holes through the UTSW down to the capture pads.

Claim 6 (currently amended): The method of claim 1 including:

initially forming capture pads on the first surface; [[,]]

then forming interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW; [[,]]

then forming the via holes through the UTSW down to the capture pads; [[,]]

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed; [[,]] and

then forming the metallization in the via holes in contact with the capture pads.

Claim 7 (currently amended): The method of claim 1 including:

initially forming capture pads on the first surface; [[,]]

then forming interconnection structure over the first surface and the capture pads

then forming the temporary bond of the wafer holder to the reverse surface; [[,]]

then thinning the wafer, thereby forming the UTSW; [[,]]

then forming the via holes through the UTSW down to the capture pads; [[,]]

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed; [[,]]

then depositing metal pads into the via holes in contact with the capture pads; [[,]] and

then [[form]] forming metal joining structures on the metal pads.

Claim 8 (previously presented): The method of claim 1 including initially forming via holes in the first surface prior to thinning the wafer.

Claim 9 (currently amended): The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer ; [[,]]

then forming a dielectric layer covering the via holes.

Claim 10 (currently amended): The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer; [[,]]

then forming a dielectric layer over the surface of the wafer including the via holes; [[,]] and

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes.

Claim 11 (currently amended): The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer; [[,]]

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes; [[,]] and

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes.

Claim 12 (currently amended): The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer; [[,]]

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes; [[,]]

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes; [[,]] and

then forming an interconnection structure over the first surface including the first metal layer.

Claim 13 (currently amended): The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer; [[,]]

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes; [[,]]

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes ; [[,[and]]

then forming interconnection structure over the first surface including the metal vias and the first metal layer; [[,]]

then forming the temporary bond to the rigid wafer holder on the reverse surface; [[,]] and

then thinning the wafer to the desired thickness of the UTSW.

CLAIMS 14-24. (CANCELLED)

Claim 25 (currently amended): A method for fabricating a Silicon Based Package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP; [[,]]

then forming an interconnection structure including multilayer conductor patterns over the first surface; [[,]]

then forming a protective overcoat layer composed of polyimide over the interconnnection structure; [[,]]

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure; [[,]]

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP; [[,]]

then forming via holes which extend through the UTSW; [[,]]

then forming metallization in the via holes with the metallization extending through the UTSW; [[,]] and

then removing the temporary bond.

Claim 26 (currently amended): The method of claim 25 including:

forming the temporary bond with polyimide; [[,]], and

releasing the temporary bond by laser ablation.

CLAIM 27. (CANCELLED)

CLAIMS 28-29. (CANCELLED)

Claim 30 (currently amended): The method of claim 1 [[29]] including the UTSW having a desired thickness including ~~the steps performed in the sequence~~ as follows:

~~performing a step of forming an interconnection structure including multilayer conductor patterns over the first surface of the silicon wafer;~~

~~then forming a protective overcoat layer over the interconnection structure;~~

[[then]] the step of forming the temporary bond between the protective overcoat layer of the SBP and the wafer holder leaving the reverse surface exposed;

~~then thinning the reverse surface of the wafer to a desired thickness to form the UTSW for the SBP;~~

~~then forming~~ the via holes ~~which extend~~ extending through the thickness of the UTSW; and

~~then forming~~ the metallization in the via holes ~~with the metallization~~ extending through the thickness of the UTSW. [[; and]]

~~thereafter releasing the temporary bond.~~

CLAIM 31. (CANCELLED)